CLAIMS

1. A circuit comprising:

a partial product generator comprising:

a first input to receive a multiplicand;

a second input to receive a multiplier;

partial product generation means for producing a plurality of partial products based on the multiplicand and the multiplier; and

an output coupled to the partial product generation means to provide the plurality of partial products; and

a partial product adder comprising:

an input coupled to the output of the partial product generator;

a plurality of adders to add the plurality of partial products to produce a final product, the plurality of adders comprising a plurality of compressors having the same width; and

an output coupled to the plurality of adders to provide the final product.

2. The circuit of claim 1, wherein the plurality of adders comprises:

an adder array comprising a subset of the plurality of adders, a first output to produce a sum signal, and a second output to produce a carry signal, the subset of the plurality of adders comprising a plurality of carry save adders to sum the plurality of partial products to produce the sum signal and the carry signal; and

a full adder comprising a first input coupled to the first output of the adder array, a second input coupled to the second output of the adder array, means for adding the sum signal to the carry signal to produce the final product, and an output to provide the final product.

3. The circuit of claim 1, wherein the multiplier is at least 64 bits wide.

4. The circuit of claim 1, wherein the multiplicand is at least 64 bits wide.

5. The circuit of claim 1, wherein the plurality of compressors are interconnected in a Wallace tree configuration.

6. The circuit of claim 1, wherein the width of each compressor *C* in the plurality of compressors is equal to the width of each of the inputs of compressor *C*.

7. The circuit of claim 1, wherein each of the plurality of partial products is at least 64 bits wide.

8. The circuit of claim 1, wherein the plurality of compressors comprises a plurality of 4-2 compressors.

9. A circuit comprising:

a partial product generator comprising:

a first input to receive a multiplicand that is at least 64 bits wide, a second input to receive a multiplier that is at least 64 bits wide;

partial product generation means for producing a plurality of partial products based on the multiplicand and the multiplier; and

an output coupled to the partial product generation means to provide the plurality of partial products; and

a partial product adder comprising:

an input coupled to the output of the partial product generator;

a plurality of adders to add the plurality of partial products to produce a final product, the plurality of adders comprising a plurality of 4-2 compressors having the same width; and

an output coupled to the plurality of adders to provide the final product.

10. A circuit comprising:

a plurality of compressors having a plurality of inputs and a plurality of outputs;

a first compressor row comprising a first subset of the plurality of compressors, the inputs of the first subset of the plurality of compressors being wired in parallel to receive a plurality of distinct inputs;

a second compressor row comprising a second subset of the plurality of compressors, outputs of the first subset of the plurality of compressors being coupled to inputs of the second subset of the plurality of compressors;

wherein all of the compressors in the plurality of compressors have substantially the same width.

11. The circuit of claim 10, wherein the width of any compressor *C* in the plurality of compressors does not differ from the width of any other one of the plurality of compressors by more than one bit.

12. The circuit of claim 10, wherein the width of any compressor *C* in the plurality of compressors does not differ from the width of any other one of the plurality of compressors by more than two bits.

13. The circuit of claim 10, further comprising:

a third compressor row comprising a third subset of the plurality of compressors, outputs of the second subset of the plurality of compressors being coupled to inputs of the third subset of the plurality of compressors.

14. The circuit of claim 13, wherein the first compressor row comprises a first compressor, a second compressor, and a third compressor, wherein the second compressor row comprises a fourth compressor, and wherein the third compressor row comprises a fifth compressor.

15. The circuit of claim 13, wherein each of the plurality of compressors is 72 bits wide.

16. The circuit of claim 10, wherein the plurality of compressors are interconnected in a Wallace tree configuration.

17. The circuit of claim 10, wherein the width of each compressor *C* in the plurality of compressors is equal to the width of each of the inputs of compressor *C*.

18. The circuit of claim 10, wherein each of the inputs of each of the plurality of compressors is at least 64 bits wide.

19. The circuit of claim 10, wherein the first compressor row comprises a first compressor, a second compressor, and a third compressor, and wherein the second compressor row comprises a fourth compressor.

20. The circuit of claim 10, wherein the plurality of compressors comprises a plurality of 4-2 compressors.

21. The circuit of claim 10, wherein the plurality of compressors comprises a plurality of carry save adders.

22. A circuit comprising:

a plurality of 72-bit wide 4-2 compressors having a plurality of inputs and a plurality of outputs, the plurality of compressors comprising a plurality of carry save adders, each of the plurality of inputs and the plurality of outputs being at least 64 bits wide;

a first compressor row comprising a first subset of the plurality of compressors, the inputs of the first subset of the plurality of compressors being wired in parallel to receive a plurality of distinct inputs;

a second compressor row comprising a second subset of the plurality of compressors, outputs of the first subset of the plurality of compressors being coupled to inputs of the second subset of the plurality of compressors; and

a third compressor row comprising a third subset of the plurality of compressors, outputs of the second subset of the plurality of compressors being coupled to inputs of the third subset of the plurality of compressors.

wherein the width of any compressor *C* in the plurality of compressors does not differ from the width of any other one of the plurality of compressors by more than three bits.

23. A circuit comprising:

a plurality of compressors having a plurality of inputs a plurality of outputs;

a first compressor row comprising a first subset of the plurality of compressors, the inputs of the first subset of the plurality of compressors being wired in parallel to receive a plurality of distinct inputs;

a second compressor row comprising a second subset of the plurality of compressors, outputs of the first subset of the plurality of compressors being coupled to inputs of the second subset of the plurality of compressors;

wherein all of the compressors in the plurality of compressors have the same width.

24. The circuit of claim 23, further comprising:

a third compressor row comprising a third subset of the plurality of compressors, outputs of the second subset of the plurality of compressors being coupled to inputs of the third subset of the plurality of compressors.

25. The circuit of claim 24, wherein the first compressor row comprises a first compressor, a second compressor, and a third compressor, wherein the second compressor row comprises a fourth compressor, and wherein the third compressor row comprises a fifth compressor.

26. The circuit of claim 24, wherein each of the plurality of compressors is 72 bits wide.

27. The circuit of claim 23, wherein the plurality of compressors are interconnected in a Wallace tree configuration.

28. The circuit of claim 23, wherein the width of each compressor *C* in the plurality of compressors is equal to the width of each of the inputs of compressor *C*.

29. The circuit of claim 23, wherein each of the inputs of each of the plurality of compressors is at least 64 bits wide.

30. The circuit of claim 23, wherein the first compressor row comprises a first compressor, a second compressor, and a third compressor, and wherein the second compressor row comprises a fourth compressor.

31. The circuit of claim 23, wherein the plurality of compressors comprises a plurality of 4-2 compressors.

32. The circuit of claim 23, wherein the plurality of compressors comprises a plurality of carry save adders.

33. A circuit comprising:

a plurality of 4-2 compressors having a plurality of inputs a plurality of outputs, each of the plurality of 4-2 compressors comprising at least one carry save adder, each of the plurality of inputs being at least 64 bits wide;

a first compressor row comprising a first subset of the plurality of 4-2 compressors, the inputs of the first subset of the plurality of 4-2 compressors being wired in parallel to receive a plurality of distinct inputs, the first compressor row comprising a first compressor, a second compressor, and a third compressor;

a second compressor row comprising a second subset of the plurality of 4-2 compressors, outputs of the first subset of the plurality of 4-2 compressors being coupled to inputs of the second subset of the plurality of 4-2 compressors, the second compressor row comprising a fourth compressor; and

a third compressor row comprising a third subset of the plurality of compressors, outputs of the second subset of the plurality of compressors being coupled to inputs of the third subset of the plurality of compressors, the third compressor row comprising a fifth compressor;

wherein all of the 4-2 compressors in the plurality of 4-2 compressors are 72 bits wide.

34. A circuit comprising:

a partial product generator comprising:

a first input to receive a multiplicand;

a second input to receive a multiplier;

partial product generation means for producing a plurality of partial products based on the multiplicand and the multiplier; and

an output coupled to the partial product generation means to provide the plurality of partial products; and

a partial product adder comprising:

an input coupled to the output of the partial product generator;

a plurality of adders to add the plurality of partial products to produce a final product, the plurality of adders comprising a plurality of compressors having substantially the same width; and

an output coupled to the plurality of adders to provide the final product.

35. The circuit of claim 34, wherein the plurality of adders comprises:

an adder array comprising a subset of the plurality of adders, a first output to produce a sum signal, and a second output to produce a carry signal, the subset of the plurality of adders comprising a plurality of carry save adders to sum the plurality of partial products to produce the sum signal and the carry signal; and

a full adder comprising a first input coupled to the first output of the adder array, a second input coupled to the second output of the adder array, means for adding the sum signal to the carry signal to produce the final product, and an output to provide the final product.

36. The circuit of claim 34, wherein the multiplier is at least 64 bits wide.

37. The circuit of claim 34, wherein the multiplicand is at least 64 bits wide.

38. The circuit of claim 34, wherein the plurality of compressors are interconnected in a Wallace tree configuration.

39. The circuit of claim 34, wherein the width of each compressor *C* in the plurality of compressors is equal to the width of each of the inputs of compressor *C*.

40. The circuit of claim 34, wherein each of the plurality of partial products is at least 64 bits wide.

41. The circuit of claim 34, wherein the plurality of compressors comprises a plurality of 4-2 compressors.

42. The circuit of claim 34, wherein the circuit comprises a first compressor row comprising a first subset of the plurality of compressors and a second compressor row comprising a second subset of the plurality of compressors, wherein compressors in the first subset have the same width as each other, and wherein compressors in the second subset have the same width as each other.

43. A circuit comprising:

a partial product generator comprising:

a first input to receive a multiplicand that is at least 64 bits wide;

a second input to receive a multiplier that is at least 64 bits wide;

partial product generation means for producing a plurality of partial products based on the multiplicand and the multiplier; and

an output coupled to the partial product generation means to provide the plurality of partial products; and

a partial product adder comprising:

an input coupled to the output of the partial product generator;

a plurality of adders to add the plurality of partial products to produce a final product, the plurality of adders comprising a plurality of 4-2 compressors having substantially the same width; and

an output coupled to the plurality of adders to provide the final product; and

a first compressor row comprising a first subset of the plurality of compressors and a second compressor row comprising a second subset of the plurality of compressors, wherein compressors in the first subset have the same width as each other, and wherein compressors in the second subset have the same width as each other.